High Speed USB Design Guidelines

1. Introduction

This document provides guidelines for integrating a AT85C51SND3Bx high speed USB device controller onto a 4-layer PCB. The material covered can be broken into two main categories: board design guidelines and layout examples.

High speed USB operation is described in the USB 2.0 Specification (http://www.usb.org/developers/docs.html).

AT85C51SND3Bx Microcontrollers

Application Note

7633A–MP3–06/06

2. Layout Guidelines

2.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality problems.

1. Place the high-speed USB host controller and major components on the unrouted board.
2. With minimum trace lengths, route high-speed clock and high-speed USB differential pairs. Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
3. Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality.
7. Route all traces over continuous GND plane with no interruptions.

2.2 High Speed USB Trace Spacing

Figure 2-1 provides an illustration of the recommended trace spacing while Table 2-1 gives some trace calculation examples. Use the following guidelines.

1. Use an impedance calculator to determine the trace width (W) and spacing (S) required for the specific board stack-up being used. W is calculated to achieve a trace impedance (Z0) of ~50W and S is calculated to achieve a differential trace impedance of 90W. These impedances depend in first approximation on the following PCB parameters delivered by the PCB manufacturer:
   - ε_r: dielectric relative permittivity
   - H: dielectric height
   - T: trace thickness
2. Maintain parallelism between USB differential signals with the trace spacing calculated to achieve 90W differential impedance. Deviations will normally occur due to package break-out and routing to connector pins. Ensure the amount and length of the deviations are kept to the minimum.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 2-1. Recommended Trace Spacing

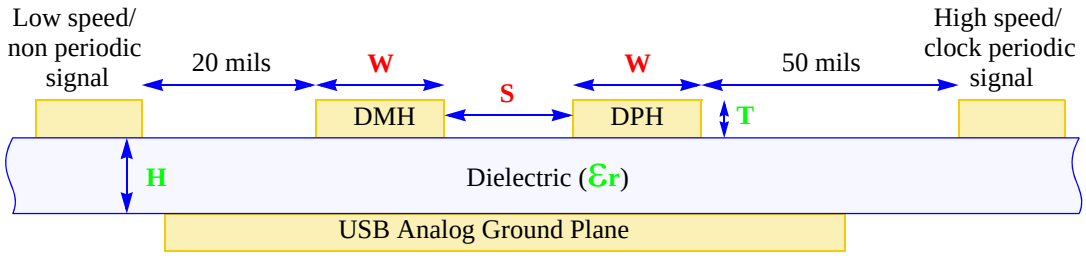


Table 2-1. Trace Characteristics Examples

PCB Characteristics			Trace Characteristics	
er	H(mils)	T(mils)	W(mils)	S(mils)
4.6	4.5	1.4	7.5	7.5
3.9	5.5	1.7	10	10

2.3 High Speed USB Termination

AT85C51SND3Bx high-speed USB design requires 39 W termination resistor at both DPH and DMH pins. Place the termination resistors as close as possible to the AT85C51SND3Bx signal pins.

2.4 High Speed USB Trace Length Matching

High-speed USB signal pair traces should be trace-length matched. Max trace-length mismatch between high-speed USB signal pairs should be no greater than 150 mils.

2.5 High Speed USB Bias Filter

AT85C51SND3Bx high-speed USB design requires a 6.81KW 1% resistor in parallel to a 10pF capacitor connected from UBIAS pin to USB ground. The resistor defines the master biasing of the AT85C51SND3Bx high-speed pad and should be placed as close as possible to the UBIAS pin by taking care to minimize noise injection at this point.

2.6 High Speed USB ESD Protection

Full-speed USB provide ESD suppression using in-line ferrites and capacitors that form a low pass filter. This technique doesn't work for high-speed USB due to the much higher signal rate of high-speed data. A recommended device that has been tested successfully is a LittelFuse® component, PulseGuard® PGB0010603MR (0603 package size). Proper placement of the devices is on the data lines as close as possible to the USB connector. Other low-capacitance ESD protection devices may work as well. We recommend including the footprints for this device, or some other proven solution, as a stuffing option in case it is needed to pass ESD testing and in the event that a problem occurs (general routing and placement guidelines should be followed).

2.7 High Speed USB Connectors

In order to provide direct connection of high-speed USB signals, we recommend to use through hole mini-AB or surface mount reversed mini-AB receptacle connector. In case AT85C51SND3Bx OTG capability is not requested, we recommend to use through hole mini-B or surface mount reversed mini-B receptacle connector or surface mount std-A plug.

3. Layout Examples

Figure 3-1 to Figure 3-3 show some examples of AT85C51SND3Bx high-speed USB routing. In order to allow direct connection to AT89C51SND3 controller, a reversed mini-AB connector is better used to avoid via and signal crossing.

Figure 3-1. Reversed Mini AB Receptacle - USB Routing Example

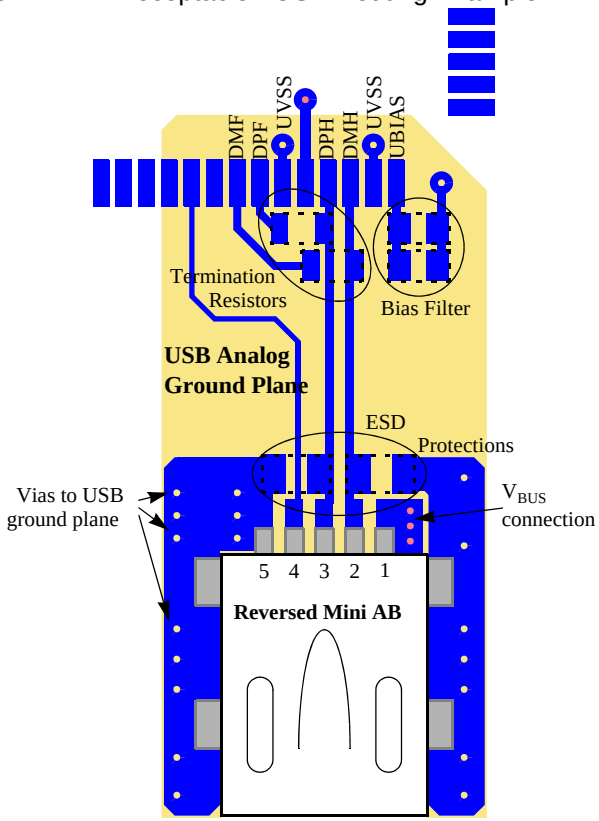


Figure 3-2. Reversed Mini AB Receptacle - USB Routing Example

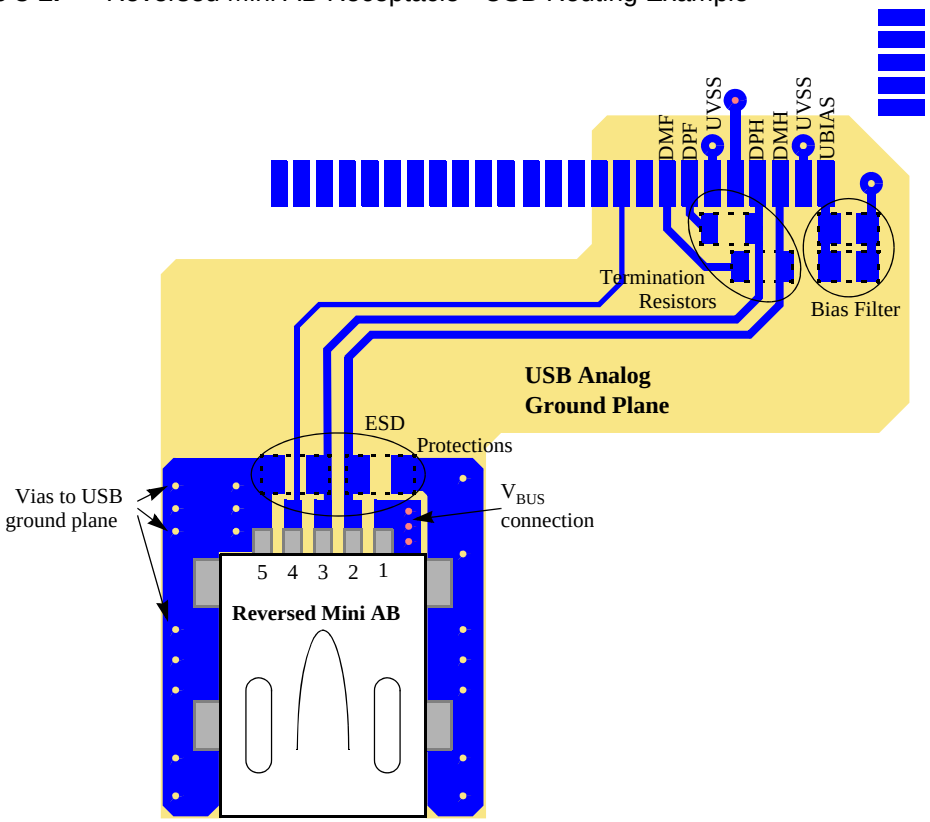


Figure 3-3. Standard Mini AB Receptacle - USB Routing Example

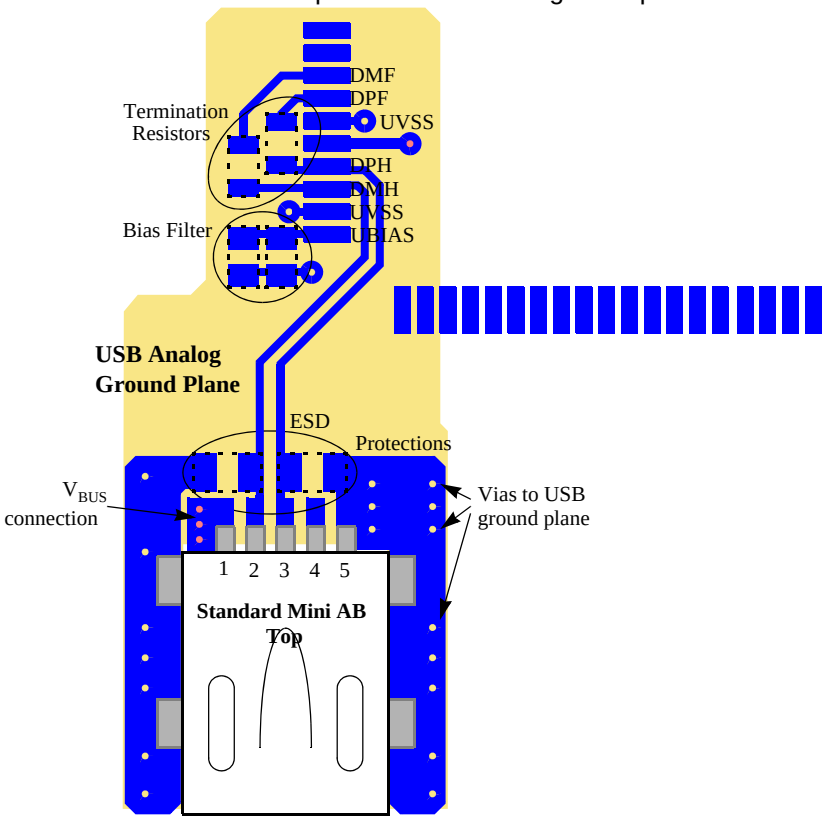
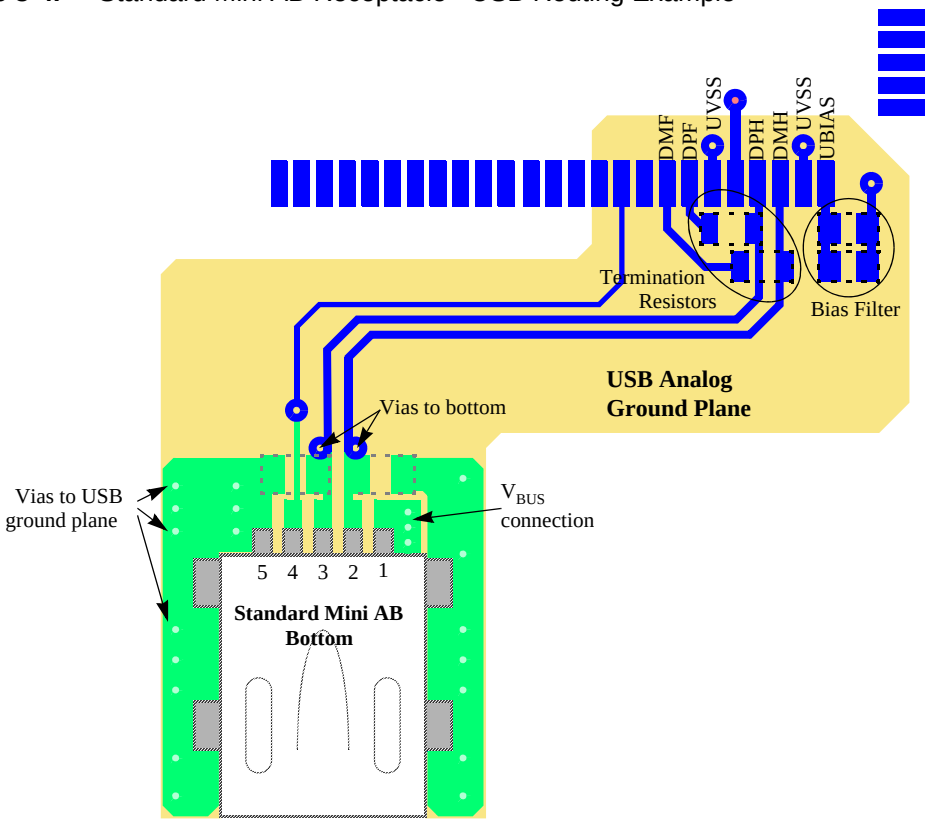


Figure 3-4. Standard Mini AB Receptacle - USB Routing Example



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7633A–MP3–06/06